Effects of postannealing on the bulk and interfacial characteristics of ZrO_2 gate dielectrics prepared on Si by metalorganic chemical vapor deposition

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This work investigates the effects of postannealing on the bulk and interfacial characteristics of ultrathin ZrO_2 films on Si substrates. The films were prepared by metalorganic chemical-vapor deposition and were subsequently annealed in N_2 or O_2 ambient at 500–900 °C. Partial crystallization of the ZrO_2 film and growth of an interfacial layer (IL) were found by the increase of the annealing temperature. The IL is mainly composed of Zr–silicate for annealing in N_2, but it is mostly SiO_2 for annealing in O_2. The annealing also effectively reduces the oxide trapped-charge density in ZrO_2, as demonstrated by the reduction of hysteresis in the capacitance–voltage relation, but not for the specimen annealed in O_2 at 900 °C, in which excessive oxygen diffused into the film and IL was found. Lower leakage current from substrate injection in association with the reduction of depletion layer, which provides less generation current, was found due to the growth of Zr–silicate IL in N_2 annealing, but the leakage from gate injection increased in conjunction with the crystallization of the ZrO_2 layer. In contrast, the relatively thick SiO_2 IL formed in O_2 annealing reduces the leakage for both substrate and gate injection. There is also a significant shift of the turn-around voltage in the current–voltage relation with voltage swept from inversion to accumulation, but not with voltage swept back. © *2004 American Vacuum Society.*
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I. INTRODUCTION

In the nanoscale low-power complementary metal–oxide–semiconductor (CMOS) technology, the use of high-κ gate dielectrics provides the solution for increasing the physical oxide thickness and maintaining a low equivalent-oxide thickness (EOT) without a remarkable increase of direct tunneling.[1] Among the many candidates, the ZrO_2 films have a combination of satisfactory properties, such as high permittivity ($\kappa \sim 24$), large conduction band offset (~1.4 eV) with Si, high stability against reaction with Si, and low leakage-current characteristics.[2] However, the ZrO_2 films appear to have a weak resistance against oxygen diffusion, which could cause the formation of a low-κ interfacial layer (IL) on the ZrO_2/Si interface during high-temperature process.[3,4] This IL plays a crucial role in CMOS performance, which exerts a fatal effect on the attempt of seeking a low EOT.[5] Moreover, the conventional dopant-activation anneals would further deteriorate the interfacial characteristics.

It has been found that the ZrO_2 would also react with the top poly-Si electrode or the bottom Si substrate, giving rise to severe degradation in leakage current and carrier mobility in the channel due to the formation of localized Zr–silicide and impurity interdiffusion from high-temperature annealing.[6–10] To overcome the earlier problems, surface modification of Si[11–13] prior to the ZrO_2 film deposition and the use of metal gates (e.g., TiN, TaN, RuO_2, Zr, etc.)[14,15] as the top electrode have been suggested. However, the postannealing treatment on improving the performance characteristics of gate dielectrics through the control of the bulk and interface structure remains to be developed. Therefore, in this work, the postannealing effect on the interfacial characteristics of the ZrO_2/Si gate stack is investigated.

II. EXPERIMENT

Metalorganic chemical vapor deposition of ZrO_2 was carried out at a substrate temperature of 275 °C using zirconium t-butoxide (ZTB) as the precursor. The ZTB was stored in a bubbler normally kept at 35 °C, but the gas lines were heated to 60 °C. High-purity argon (99.999%) at a gas-flow rate of ~50 sccm was used to carry the ZTB vapor into the reaction chamber to react with high-purity oxygen of ~40 sccm at a pressure of 2 Torr for 1 min. 6-nm-thick ZrO_2 film was prepared on the HF-last *p*-type Si (100) substrate, followed by rapid thermal annealing in N_2 (RTN) or O_2 (RTO) ambient at temperatures from 500 to 900 °C for 30 s.

The total thickness and refractive index (n) of the ZrO_2 thin film, including the IL on Si substrate, were evaluated from spectroscopy ellipsometry (S–E) with a single layer mode at a fixed angle of ~70° and a wave length of 400–800 nm. Cross-sectional high-resolution transmission electron microscopy (HRTEM) was employed to examine the thickness and microstructure of ZrO_2 and IL. The chemical-binding states were also investigated by x-ray photoelectron spectroscopy (XPS) with monochromatic Mg

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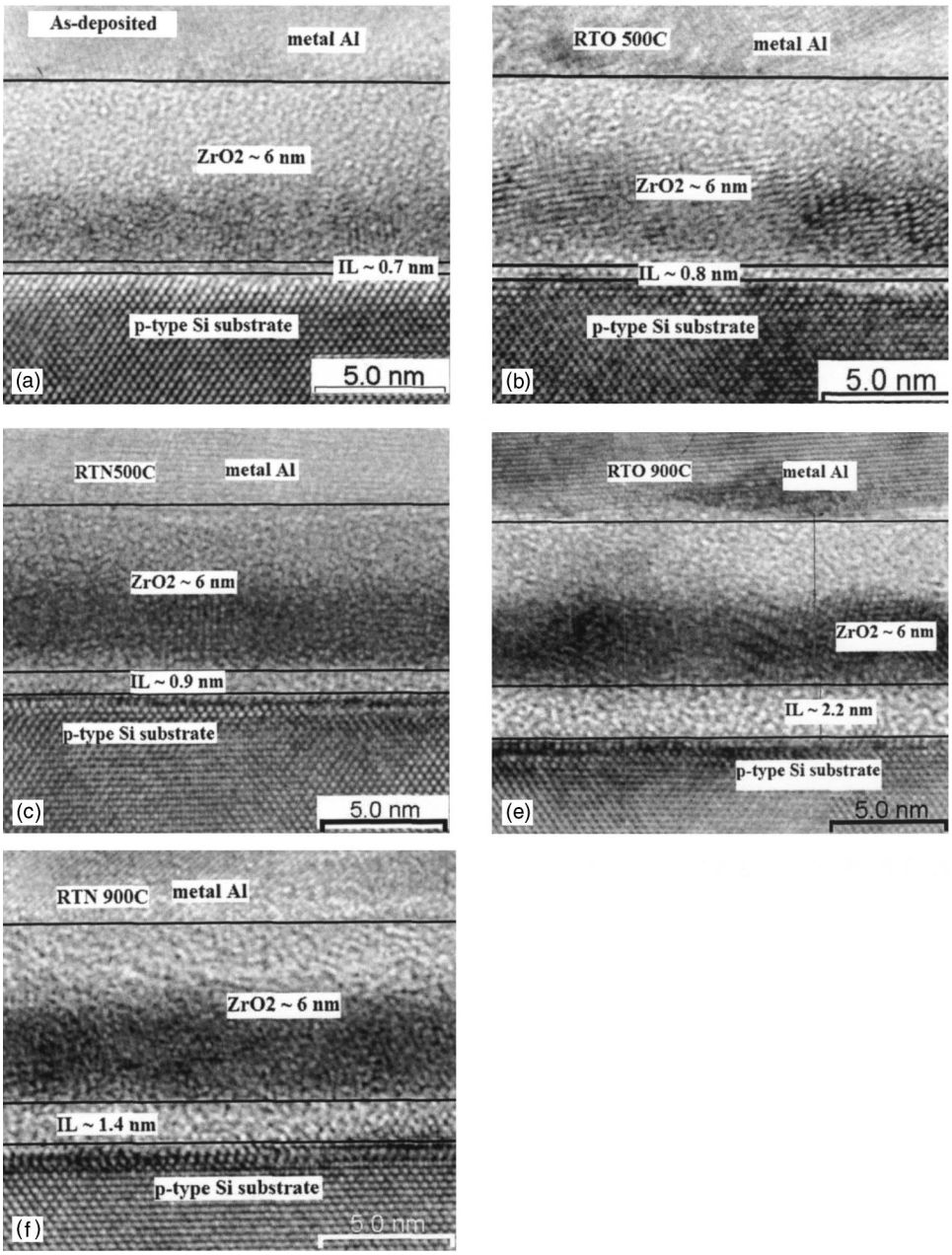

FIG. 1. Cross-sectional HRTEM images of the 6-nm-thick ZrO_2/interfacial layer/p-Si stack with a metal Al cap layer, including (a) the as-deposited, and those annealed with (b) RTN 500 °C, (c) RTN 900 °C, (d) RTO 500 °C, and (e) RTO 900 °C, respectively.

($K\alpha$) x-ray radiation at a take-off angle of 54° and a reference binding energy (BE) at 99.2 eV from the Si^0 ($2p$) peak position was used. Finally, the depth profiles of carbon (C), hydrogen (H), and oxygen (O) were measured by secondary ion mass spectroscopy (SIMS) with positively secondary-ion (Cs^+) detection mode and monitoring CsX^+ clusters at the oblique angle of ~45°. The analysis beam of ~10 keV and sputtering beam of ~5 keV were rastered on a 50×50 $(\mu m)^2$ and 100×100 $(\mu m)^2$ area, respectively.

For electrical property measurements, the $Al/ZrO_2/p$-Si/Al MOS capacitors were fabricated by thermal evaporation of Al as the top electrode, and an ohmic contact was also made on the back of Si substrate. The capacitance–voltage (C–V) relation was then measured with HP 4284A at 1 MHz by voltage sweeping from accumulation to inversion, and then sweeping back. Finally, the current–voltage (I–V) relation was measured with a HP 4140B PA meter using a stair-sweep-voltage mode with a step height of 0.1 V. All the measurements were carried out at room temperature.

III. RESULTS AND DISCUSSION

Figure 1 shows the cross-sectional HRTEM micrographs of ZrO_2/Si stacks before and after postannealing. An ~0.7 -nm-thick IL can be observed in the as-deposited film and the IL grows to ~1.4 and ~2.2 nm thick after annealing at

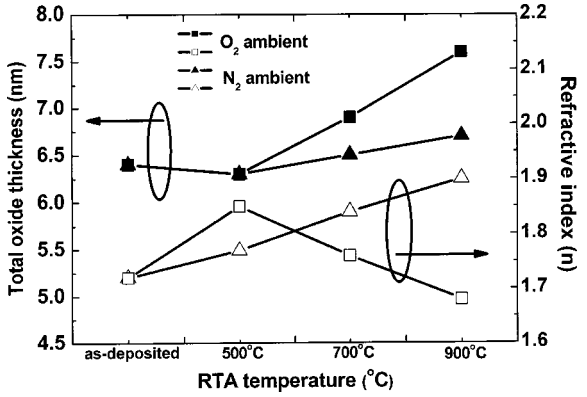

FIG. 2. Thickness and refractive index (n) of the total oxide film, before and after annealing, evaluated from the $S-E$ measurement.

900 °C in N_2 and O_2, respectively. It is also found that the amorphous ZrO_2 becomes partially crystallized after annealing. Figure 2 shows that the change of refractive index (n) and the total thickness, obtained from $S-E$ measurement, of the oxide film on Si as a function of postannealing temperature. Since the ZrO_2 layer has a nearly fixed thickness around 6 nm, the increase of the total oxide thickness corresponds to the growth of IL after annealing. As shown in Fig. 2, the IL grows very slowly for annealing in N_2 (RTN) up to 900 °C, but the value of n increases from 1.72 to 1.90. The increase in the value of n implies the densification and crystallization of the ZrO_2 film. However, the reported refractive indices of crystalline ZrO_2 ($n=2.19$ for cubic, 2.16 for tetragonal, and 2.24 for monoclinic phase)[16] are higher than those found here ($n \leqq 1.90$), which is obviously due to the incomplete crystallization of the ZrO_2 after RTN annealing, as observed from the previous HRTEM result. On the other hand, for annealing in O_2 (RTO), a significant growth of the IL occurs at temperature above 700 °C, which is apparently related to the oxidation of Si substrate by the inward-diffusion of oxygen from the O_2 ambient. It is also interesting to notice that the value of n first increases and then decreases with increasing the annealing temperature. The initial increase of n value is most likely due to the densification and crystallization of ZrO_2 films, but the latter decrease should be attributed to the growth of IL with a low refractive index.

In order to find out the chemical-binding states in the ZrO_2 and IL, the XPS is then employed. Figures 3(a) and 3(b) show the Si ($2p$) spectra of the ZrO_2/Si stacks annealed in N_2 and O_2. For RTN annealing, the spectra exhibits a constant Si^0 ($2p$) BE at 99.2 eV, but the peak of SiO_x at 103 eV gradually shifts to 102.5 eV, which corresponds to the BE of Zr–silicate, with the increase of the annealing temperature to 900 °C. This indicates that the IL formed in RTN annealing is mostly the Zr–silicate. In addition, the peak of silicon dioxide (O–Si–O) at 103.5 eV is not found in any of the scans. For RTO annealing, however, an opposite direction of peak shift is observed from the BE of SiO_x at 103 eV to that of SiO_2 at 103.5 eV along with an increase in peak intensity. This suggests that the IL formed in RTO annealing

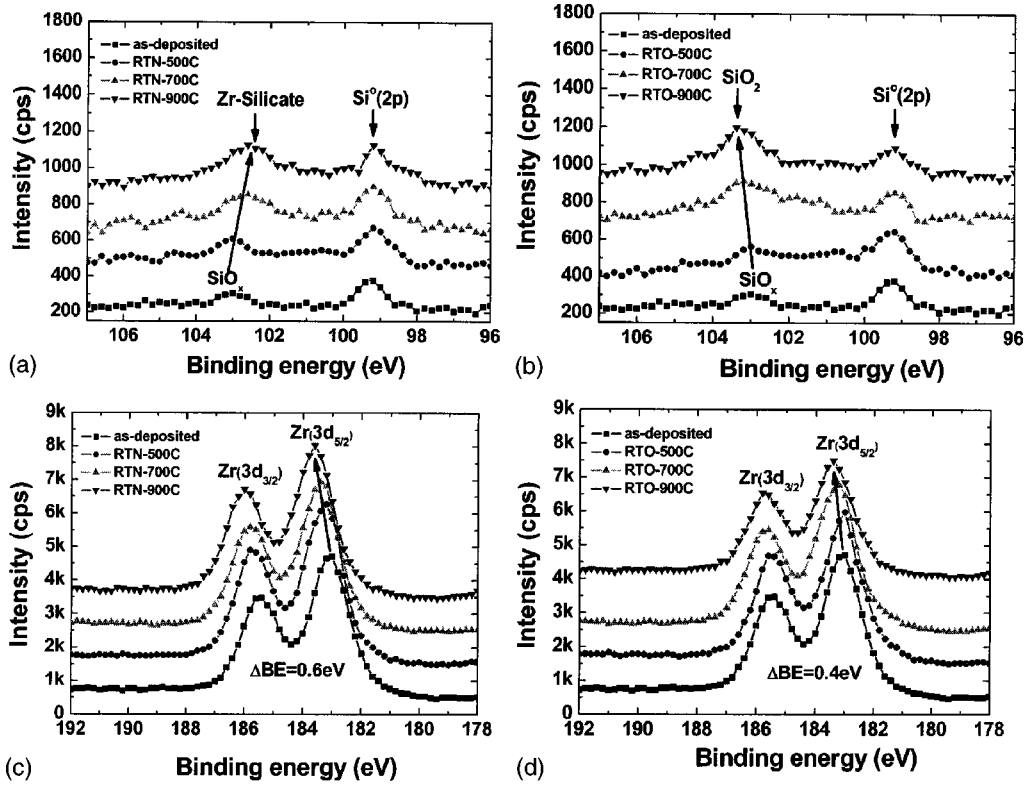

FIG. 3. Si ($2p$) spectra of XPS from specimens subjected to (a) RTN and (b) RTO annealing, and the Zr ($3d$) from (c) RTN and (d) RTO annealing, respectively.

is mainly SiO_2. The measured BE shift between Zr–silicate and SiO_2 in the earlier two cases is ~1.0 eV, which is consistent with the theoretical value of ~1.1 eV.[17] Figures 3(c) and 3(d) show the Zr ($3d$) spectra of the earlier-mentioned specimens, which are split into two spin-orbit components, $3d_{5/2}$ and $3d_{3/2}$, separated by ~2.4 eV. The measured BE of Zr ($3d_{5/2}$) in the as-deposited ZrO_2 film is around 183 eV, which corresponds to the fully oxidized state of zirconium, i.e., Zr^{4+}. As shown in Fig. 3(c), along with the increase of RTN temperature, the BE of Zr ($3d_{5/2}$) gradually increases from 183 to 183.6 eV. Consistent with the previously observed BE shift of the peak from SiO_x toward Zr–silicate, this shift of BE ($\Delta BE \sim 0.6$ eV) also suggests the formation of Zr–silicate since the BE of Zr ($3d_{5/2}$) in $ZrSiO_4$ is ~184.5 eV. However, the BE shift in O_2 annealing is somewhat smaller ($\Delta BE < 0.4$ eV), as shown in Fig. 3(d). It implies that less Zr–silicate is formed in RTO annealing. Moreover, there is no any signal of the peak from Zr–silicide ($ZrSi_x$) (BE ~ 179 eV) was found in all spectra of the annealed specimens.

The SIMS depth profiles of the C, H, and O in the as-deposited and annealed ZrO_2 films are shown in Fig. 4. It can be seen from Figs. 4(a)–4(d) that both C and H contaminations from the Zr precursor are reduced as the annealing temperature increases, and they are more effectively eliminated by O_2 annealing. On the other hand, the oxygen profiles shown in Figs. 4(e) and 4(f) reveal that there is a slight decrease of oxygen in the N_2-annealed specimens, but oxygen increases in the O_2-annealed specimens. This suggests that mobile oxygen species may depart from the ZrO_2 films in RTN, but diffuse into the ZrO_2 films in RTO. Moreover, the oxygen signal is reduced in annealing in N_2, but the signal is greatly enhanced in the IL in annealing in O_2, especially at 900 °C. All this indicates that the mobile oxygen from O_2 ambient can freely diffuse through the ZrO_2 and excessively reside in the IL.

Figure 5 shows the high frequency $C-V$ relations of the $Al/ZrO_2/Si$ MOS capacitors with voltage swept from accumulation to inversion. A counterclockwise hysteresis at flatband is observed in the $C-V$ curves, and the hysteresis, ΔV_{FB}(hys), decreases from ~0.22 V to ~2 mV as the annealing temperature increases except the curve from RTO at 900 °C, as shown in the upper insets. The suppression of hysteresis indicates that the density of trapped-charge defects in the ZrO_2/Si stack is reduced by annealing. It is most likely related to the annihilation of residual carbon and hydrogen species from the metalorganic precursor in the as-deposited ZrO_2 film. As for RTO at 900 °C, however, the increase of ΔV_{FB}(hys) suggests that oxygen-related defects, such as interstitial oxygen, $[O_i]^-$, may be formed from the excess oxygen diffused into the ZrO_2 and IL. It is also observed that the stretch-out of $C-V$ curves along the voltage axis decreases with the increase of the annealing temperature, implying a reduction of the interface-trapped density (D_{it}) at midgap.[18,19] Moreover, the 500 °C-annealed specimens, either in N_2 or O_2, exhibit a maximum capacitance in the strong accumulation regime, and, in association with the thickening of interfacial layers, the capacitance value decreases with increasing the annealing temperature over 700 °C. The variations of the depletion width estimated from the strong inversion regime at 2 V are also shown in the lower insets of Fig. 5. The depletion decreases with increasing the annealing temperature either in N_2 or O_2, which is apparently due to the decrease of applied field in the capacitors associated with the thickening of interfacial layers.

The EOT and effective dielectric constant (κ_{eff}) of the ZrO_2/Si stacks, evaluated from the earlier $C-V$ curves, are shown in Fig. 6. The initial decrease of EOT (or increase of κ_{eff}) along with the increase of the annealing temperature corresponds to the densification and crystallization of the ZrO_2 film, but the later increase is apparently related to the growth of low-κ IL, as observed from the previous $S-E$ and HRTEM results. Moreover, since the IL formed in RTO is mainly SiO_2, which has a lower dielectric constant than that of Zr–silicate formed in RTN, a larger increase of EOT results is found in RTO. Figure 7 shows the change of flatband capacitance (C_{FB}) and voltage (V_{FB}) against the annealing temperature. The flatband voltage, V_{FB}, is always negative, indicating the presence of positively charged defects, most likely the overcoordinated oxygen defects such as $[Si_2=OH]^+$ and $[Zr_2=OH]^+$,[20,21] in the ZrO_2/Si stacks. For annealing in N_2, the V_{FB} value only slightly changes from −1.11 to −1.17 V, and the C_{FB} is also insignificantly affected. The result clearly demonstrates the stable characteristics of both ZrO_2 film and Zr–silicate IL from N_2 annealing. However, the V_{FB} and C_{FB} exhibit larger sensitivity to annealing in O_2. The V_{FB} first shifts to a higher negative voltage and then moves to a lower value along the increase of the annealing temperature to 900 °C. The negative shift of V_{FB} suggests the increase of the positively charged overcoordinated oxygen defects in the ZrO_2/Si stacks by annealing in O_2 at temperatures ≦700 °C. However, with further increasing the temperature to 900 °C, the overcoordinated defects can be repaired and replaced by the negatively charged defects of interstitial oxygen, $[O_i]^-$, due to the excess oxygen diffused into the ZrO_2 and IL. Consequently, a positive shift of V_{FB} would occur.

Figure 8 shows the polarity dependence of leakage current in the ZrO_2/Si stack. For the specimens annealed in N_2, the saturated leakage current from substrate injection at positive gate voltage gradually decreases along with the increase of the annealing temperature. The leakage current on the inversion condition is mainly limited by the supply of minority carriers (electrons) generated from the depletion region.[22–26] Therefore, the reduction of substrate injection is most likely related to the lower generation current due to the less depletion in the capacitors containing a thicker IL, as observed previously in the insets of Fig. 5. In contrast, the saturated leakage current from gate injection at negative gate voltage increases with the increase of the annealing temperature, but it slows down for annealing above 500 °C. The abrupt change of leakage after annealing is probably associated with the crystallization of the ZrO_2 film, which can provide grain boundaries as the fast leakage path giving rise to a higher

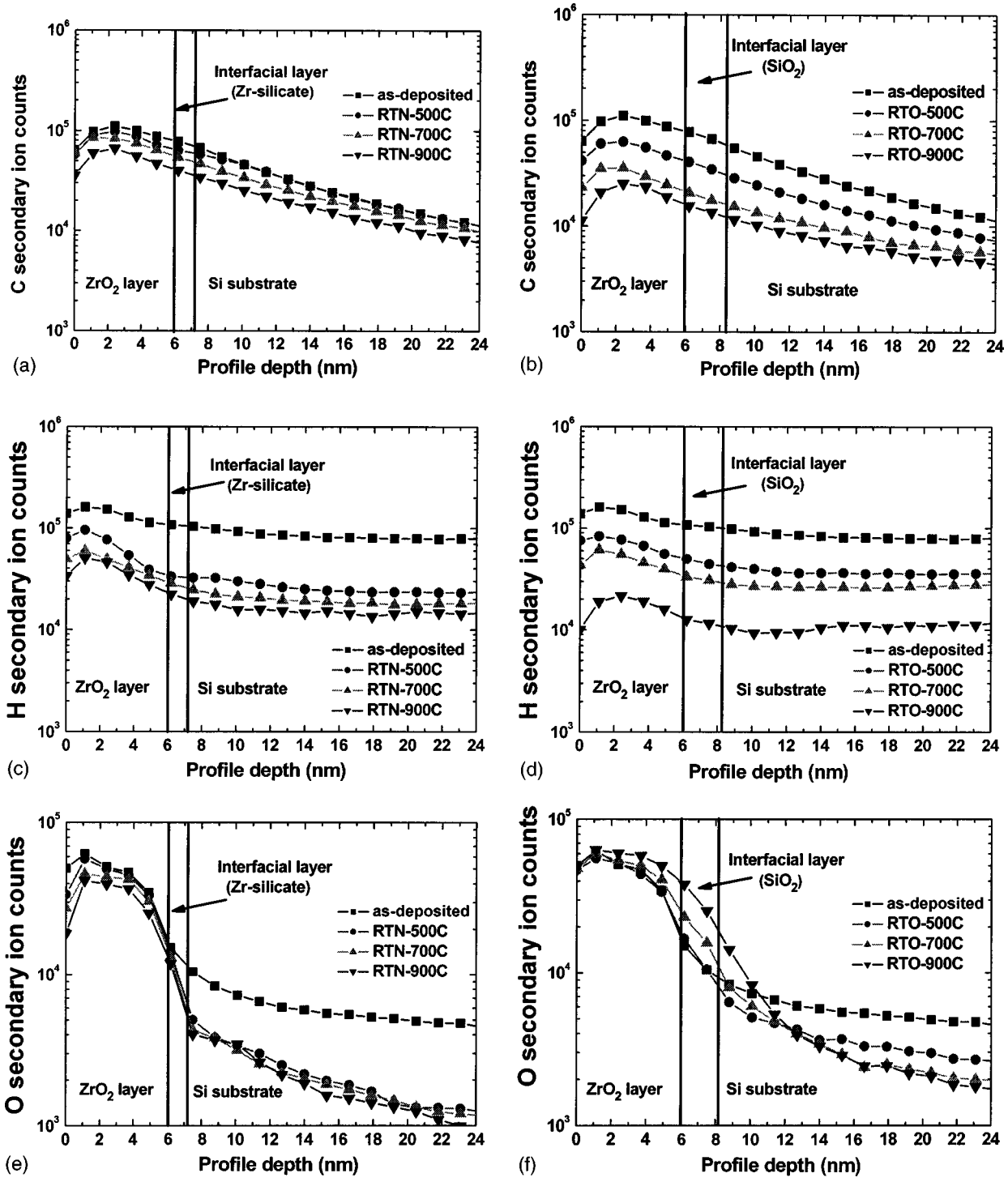

FIG. 4. SIMS depth profiles of C [(a) and (b)], H [(c) and (d)], and O [(e) and (f)] in specimens before and after annealing.

leakage over the barrier of thin Zr–silicate IL. On the other hand, for the specimens annealed in O_2, the leakage from substrate injection is similarly reduced with the increase of the annealing temperature due to the decrease of depletion in association with the thickening of IL. However, the leakage from gate injection increases first for annealing at 500 °C, and then becomes greatly decreased for annealing at higher temperatures. It is apparently due to the growth of much thicker SiO_2 IL in the MOS structure, which effectively suppresses the leakage from the crystallized ZrO_2 layer.

It is also noticed from Fig. 8 that there is a shift of turnaround voltage, V_t, which is defined at the gate voltage where the sign of the leakage current changes. The V_t measured from the current–voltage relation with voltage swept from accumulation to inversion (positive-sweeping) and the reverse (negative-sweeping) of all the specimens are also

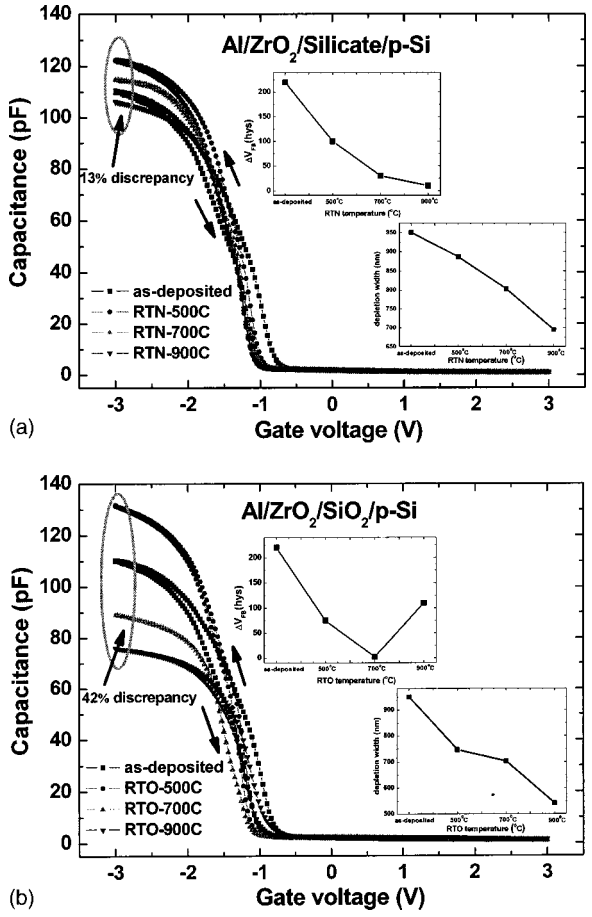

FIG. 5. High frequency capacitance–voltage relations of the $Al/ZrO_2/IL/Si$ stacks: (a) annealed in RTN, and (b) annealed in RTO; the insets show the change of hysteresis at flatband and the variation of depletion width.

shown in the insets of the figure. It is interesting that the shift of V_t under the negative-sweeping condition is quite significant, and a drastic shift is found from the specimen in RTO at 900 °C. It has been suggested that the shift of V_t is related to the trapped electrons at the inner-interface state.[27] For RTN annealing, the measured V_t values under negative-sweeping condition are all around 0.5 *V*. This reveals that the

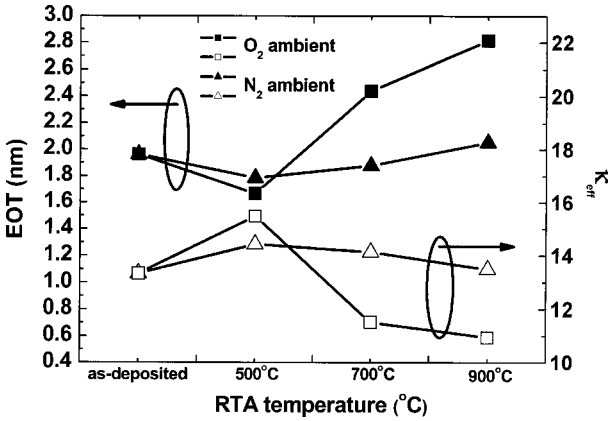

FIG. 6. EOT and effective dielectric constant (κ_{eff}) of ZrO_2/Si stacks annealed in N_2 or O_2 ambient.

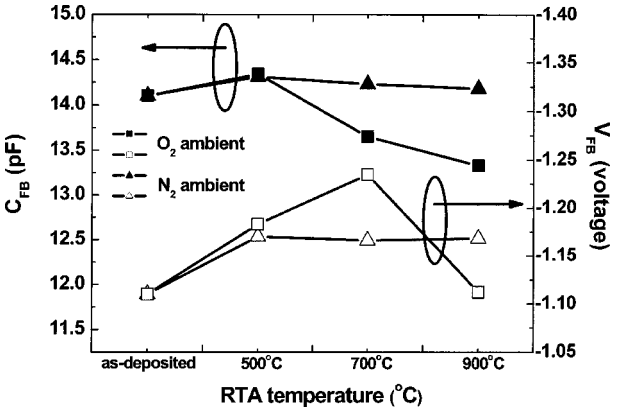

FIG. 7. Flatband capacitance (C_{FB}) and voltage (V_{FB}) of ZrO_2/Si stacks annealed in N_2 or O_2 ambient.

annealing insignificantly affects the density of the inner-interface state for electron trapping. Similar conclusion can also be obtained with RTO below 700 °C. As for the large shift of V_t from RTO at 900 °C, it may be related to the extra contribution of the excessive oxygen defects formed in the

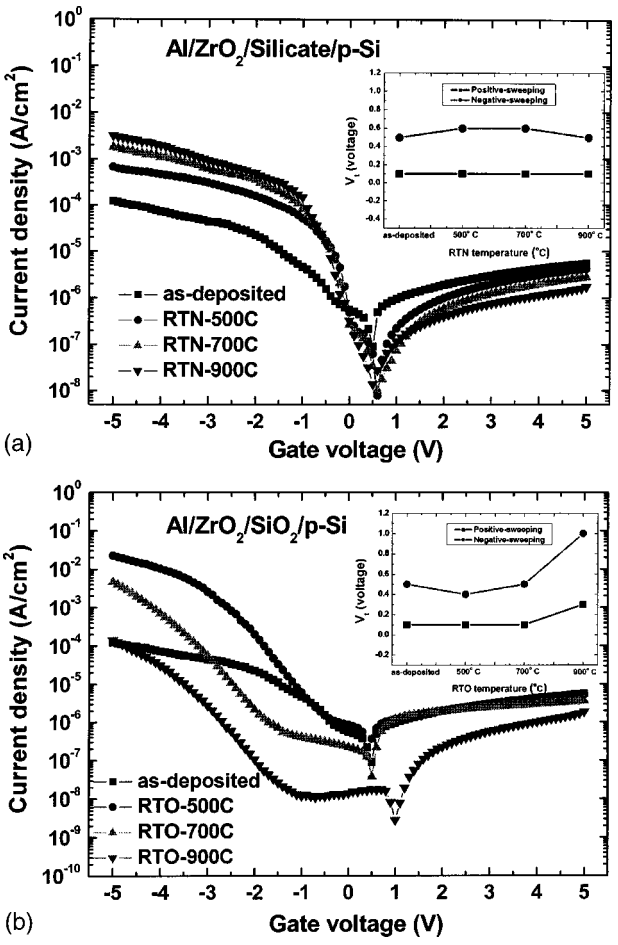

FIG. 8. *I–V* characteristics of the $Al/ZrO_2/IL/Si$ stacks with voltage swept from inversion to accumulation (negative-sweeping): (a) annealed in RTN and (b) annealed in RTO; the insets show the turn-around voltage measured from the *I–V* relations.

ZrO_2 and IL. On the other hand, for the voltage swept from accumulation to inversion (positive-sweeping), the small V_t of $\sim$0.1 V in all the specimens implies that the trapping of holes is unlikely to occur at the inner-interface states.

IV. CONCLUSION

The 6 nm thick ZrO_2 films were prepared on Si substrate by MOCVD and annealed in N_2 or O_2 ambient at 500–900 °C. A thin IL of SiO_x was formed in the as-grown ZrO_2 on Si, and partial crystallization of the films was found after annealing. The thin IL also transforms from SiO_x into Zr–silicate and slowly grows for annealing in N_2. However, the IL changes into SiO_2 and grows quite rapidly by annealing in O_2. The different ILs formed in the ZrO_2/Si stack strongly affect its electrical characteristics. Counterclockwise hysteresis was found in the $C-V$ relation and it decreases with increasing the annealing temperature except for the one from annealing in O_2 at 900 °C. The corresponding EOT first decreases for annealing at 500 °C to a value around 1.7 nm, and, then, increases with annealing at higher temperatures. However, the annealing in O_2 would cause the increase of EOT more significantly. The $I-V$ relation reveals that the saturated leakage current from substrate injection decreases with increasing the annealing temperature either in N_2 or O_2. However, the leakage from gate injection increases for annealing in N_2, but the leakage first increases and then decreases for annealing in O_2. It is also observed that there is a significant shift of the turn-around voltage in the $I-V$ relation with voltage swept from inversion to accumulation, but not with voltage swept back.

ACKNOWLEDGMENT

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